* R M - 7 1 0 1 / 8 0 0 *

RM-7101

B. E. III (Sem. VI) (Ele.) Examination

May / June – 2010

Pulse & Linear Circuit

Time : **3** Hours] [Total Marks : **100**

Instruction :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ **B. E. 3 (Sem. 6) (Electrical)**

Name of the Subject :

☛ **Pulse & Linear Circuit**

☛Subject Code No. : **7 1 0 1** ☛Section No. (1, 2,.....) : **1&2**

Seat No. :

Student's Signature

(2) Attempt all questions.
(3) Figures to the **right** indicate full marks.
(4) Assume suitable data wherever required.
(5) Write answers of both sections in **separate** answer books.

SECTION - I

1 (a) Attempt any **five** : **10**

(i) What are the important characteristics of the comparator?

(ii) What is frequency stability in oscillator? Explain its significance.

(iii) Define : (i) CMRR and (ii) Output voltage swing.

(iv) (a) The output offset voltage is the dc voltage that at the output of the op-amp when both inputs are grounded. - True/False.

(b) The higher the value of SVRR, better the op-amp performance - True/False.

(v) State the ideal op-amp characteristics.

(vi) What is virtual ground?

(b) Identify the given circuit and draw the output waveform for the given input waveform : (**Fig.1**) **3**

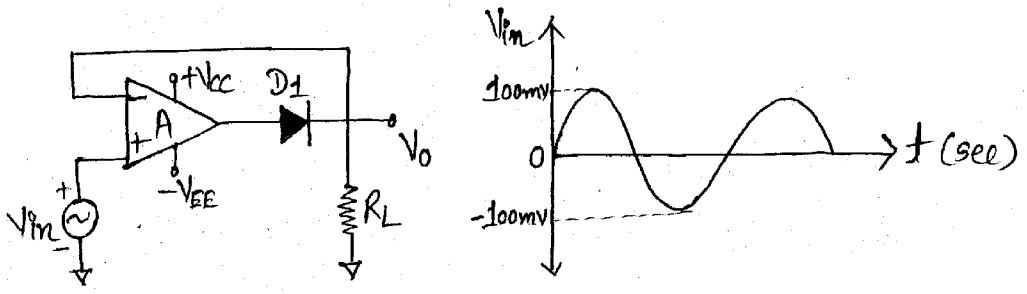

Fig. 1

(c) Match the following : 4

A	*B*
(i) Input offset current	(i) $\frac{I_{B1}+I_{B2}}{2}$, when $V_0 = 0$
(ii) PSRR	(ii) $\frac{dV_0}{dt}$ / maximum
(iii) Input bias current	(iii) $\frac{\Delta V_{io}}{\Delta V_{CC}}$
(iv) slew rate	(iv) $\lvert I_{B1} - I_{B2} \rvert$, when $V_0 = 0$

2 (a) Design all pass filter for phase shift of 90° with circuit diagram and waveforms. Assume frequency of signal as 1 kHz. 8

(b) For the circuit shown in figure=2 find the output voltage when: 7

(i) $R_1 = R_2 = R_3 = R_4 = 2\ K\ \Omega$ and

(ii) $R_1 = R_2 = R_3 = 2\ K\ \Omega$ and $R_4 = 2.2\ K\ \Omega$.

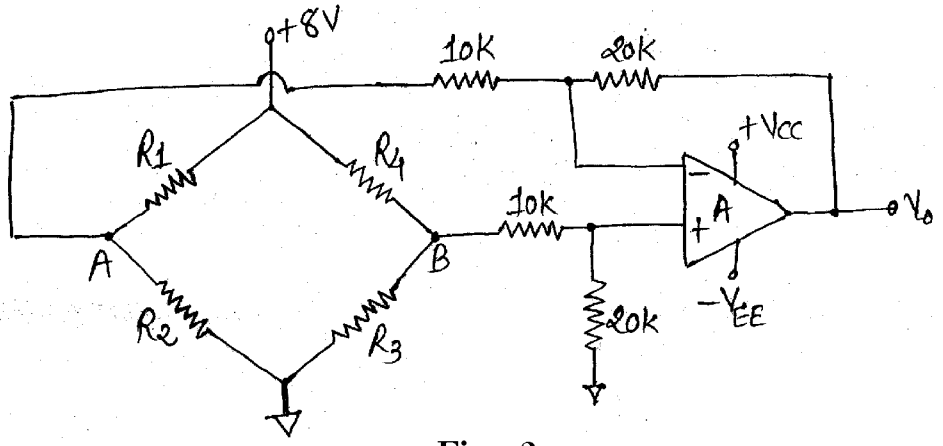

Fig. 2

OR

2 (a) Explain the monostable multivibrator using op-amp and obtain the expression for the output pulse width. 8

(b) For the circuit shown in Figure 3 find the value of R_1, so that $V_2 = -100V_1$ if R = 10 K Ω . 7

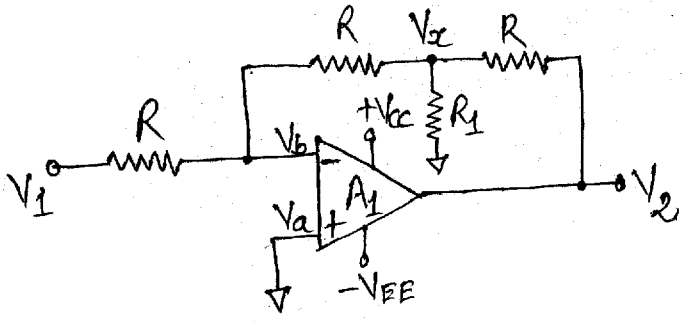

Fig. 3

3 Attempt any **three** : 18

(i) Op-amp as summing, scaling and averaging amplifier for closed loop inverting configuration.

(ii) Wein bridge oscillator using op-amp.

(iii) Bistable multivibrator using op-amp.

(iv) Peak detector

(v) Schmitt trigger.

SECTION - II

4 (a) Answer the following questions :

(i) Pin No. 4 of 555 timer is generally connected with V_{CC}. True/False. 1

(ii) Three-terminal voltage regulator can be used as a constant current source. True/False. 1

(iii) Explain current hogging. 2

(iv) If a linear regulator output voltage has a change of 0.06 V for an input voltage change of 4V, then % line regulation is _____. 2

(v) Define following terms :

(a) Propagation delay 1

(b) Fold back current limiting 1

(c) Safe Operating Area (SOA) 2

(b) (i) Explain two input TTL NAND gate. 6

(ii) The drain current of MOS device generally depends on which parameters? Explain in brief. 4

5 (a) Describe the hysterisis effect of 555 timer IC with input and output waveforms. **7**

(b) Explain working of DTL NAND gate. What is the drawback and how it can be improved? **8**

OR

5 (a) Explain in detail the application of 555 timer as a monostable multivibrator. **8**

(b) Explain three terminal voltage regulator. How current boosting can be done? **7**

6 Attempt any **three** : **15**

(i) Explain the working of PLL along with its block diagram.

(ii) Working of two input RTL NOR gate.

(iii) Write a short note on SMPS.

(iv) Design a divide by 5 circuit to obtain 2 kHz square waveform from pulses of frequency 10 kHz. Use 555 timer. Take C = 0.01 μF.